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intacs® Hardware SPICE

intacs® Working Group ‘Hardware SPICE’

Attila FEHÉRVÁRI

Head of the Hardware SPICE working group

intacs® AT/BG/CZ/HR/HU/SI/RS Regional Event in Budapest 14-15.05.2025

Principal Assessor & Instructor

Attila FEHÉRVÁRI

- *intacs Principal Assessor and Instructor (Automotive SPICE),*
- *Leader of the intacs® Hardware SPICE PAM/PRM definition workgroup,*
- *Member of the VDA-AK13 “Automotive SPICE”,*

- *Many-many years experience with VW standards (as part of the department for defining them),*
- *Project- and Process management,*
- *More than 20 Years of System and Software development.*

Agenda

1) **History of Hardware SPICE**
2) Constraints, inputs and motivations
3) Scope and terminology
4) The four processes
5) Achievements and future

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Then and now

Automotive SPICE® 2.5 (2010)
covers only the system and software domains

Nov 2019
Hardware PRM/PAM 1.0
(as a plug-in proposal)

Automotive SPICE® 3.0 (2015), **3.1**(2017)
still, only the SYS and SWE domains are covered

However, allows for “plug-in" sub-domains such as hardware or mechanical.

Dec 2020
intacs **Hardware SPICE 2.0**
incl. functional safety remarks and notes

Nov 2023
intacs **Hardware SPICE 3.0**
incl. functional safety remarks and notes

Nov 2023
Automotive SPICE 4.0 released, Hardware Engineering Processes are included.

Summer 2025
intacs **Hardware SPICE**
includes functional safety, and includes cybersecurity remarks and notes

intacs® working group “Hardware SPICE”

- Feb 2018: working group "Hardware Engineering Processes" established
  - Goal: support the growing need for
    - ISO/IEC 330xx-compliant PRM & PAM for electrical/electronic hardware development
    - also serving as a “plug-in” proposal for Automotive SPICE® v3.1
- 1st release Hardware Engineering PRM/PAM: Nov 2019
- 2nd release Hardware SPICE PRM/PAM: Dec 2020
- 3rd release Hardware SPICE PRM/PAM: Nov 2023
  - Upgrades according to Automotive SPICE 4.0
- 4th release Hardware SPICE PRM/PAM: this Summer
  - Upgrades according to Automotive SPICE 4.1

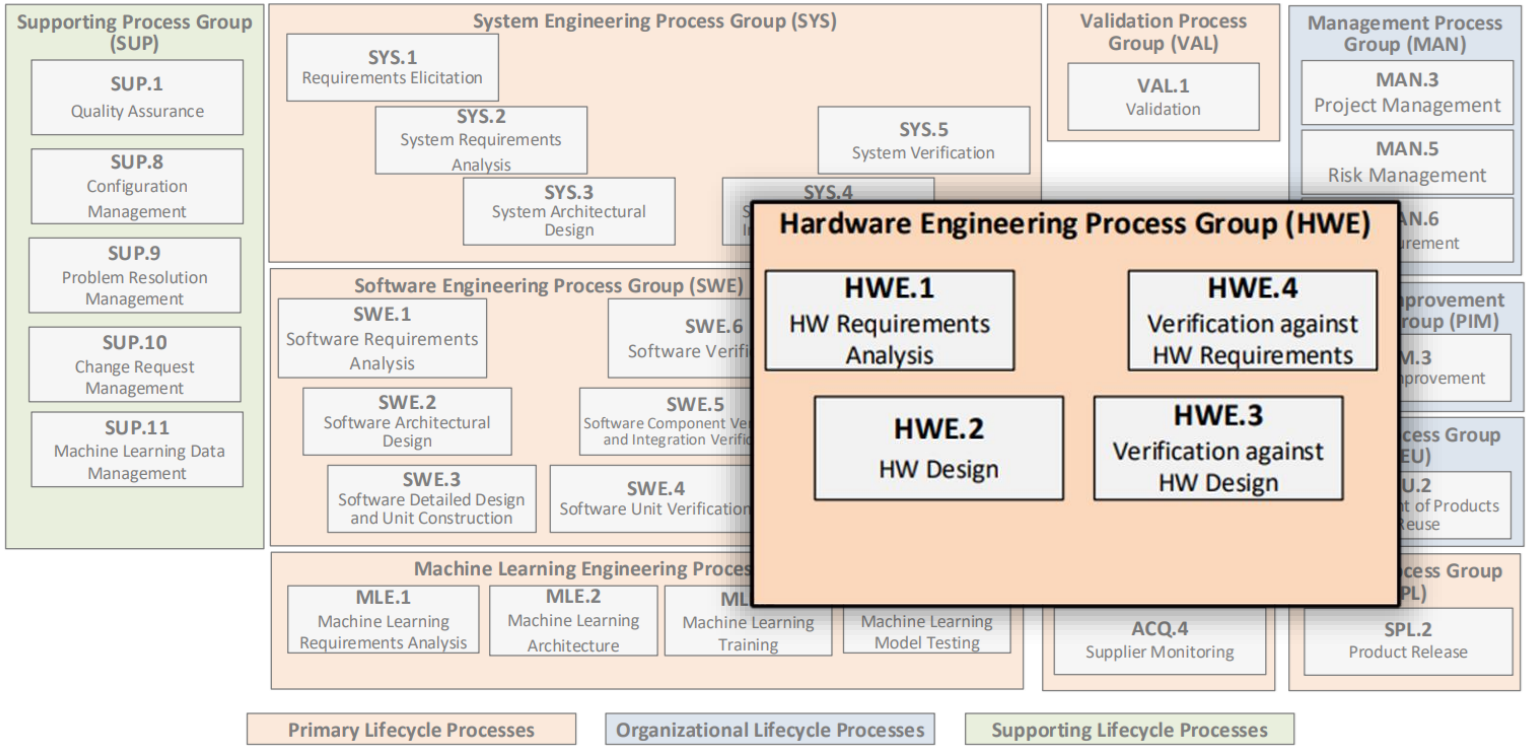
Hardware Engineering Process Group vs. intacs Hardware SPICE

Automotive SPICE®

Process Reference Model

Process Assessment Model

Version 4.0



Hardware SPICE

HWE.1
Hardware Requirements Analysis

HWE.2
Hardware Design

HWE.3
Verification against Hardware design

HWE.4
Verification against Hardware Requirements

HW-Notes

Functional Safety

Cybersecurity

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1) History of Hardware SPICE
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Constraints, inputs and motivations

- Semiconductor manufacturer perspective
- Controller device supplier perspective

- Automotive SPICE® PRM/PAM v3.1
- VDA BlueGoldBook “Automotive SPICE® Guidelines” v1.0
- ISO 26262:2018

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Result

- Base Practices and Notes
- Examples in notes
- Rating Rules together with the PRM/PAM
- Cross-references to ISO 26262 process clauses
- Rationales for key concepts

- Automotive SPICE®, including the hardware processes in version 4.0

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1) History of Hardware SPICE
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Technical Scope of the PRM/PAM (1/3)

- Development of pure electrical or electronic hardware engineering

- Excluding:
  - system level engineering (i.e., not mechatronic or ECU level)
  - mechanical aspects (e.g., housing)
  - mechanical or hardware sample manufacturing
  - supply chain
  - procurement
  - production

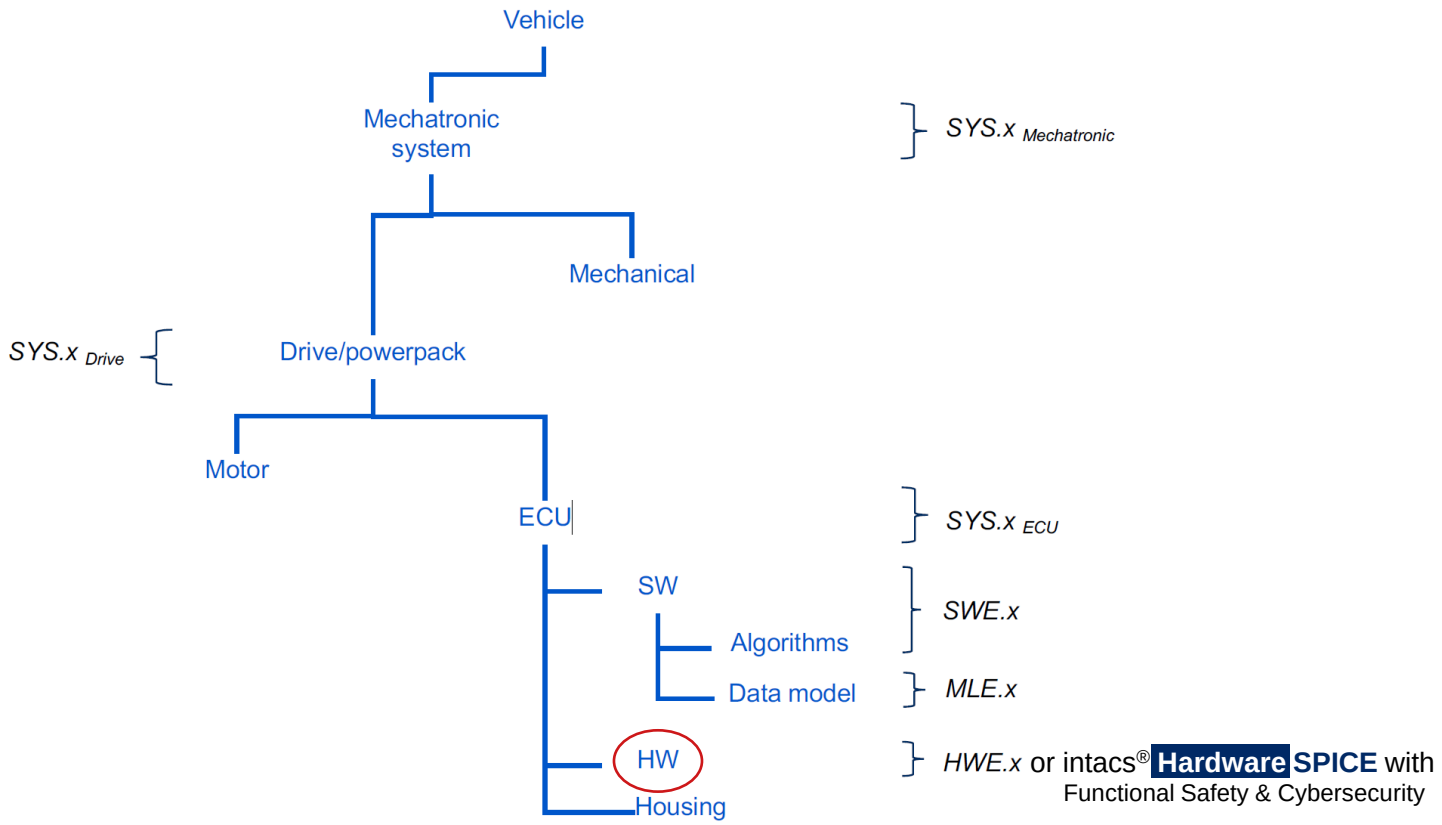
➔ However, process interfaces are included to
  - procurement
  - production and prototype/sample workshops

Receiving physical design-compliant hardware parts for verification / testing

Providing information such as production data and requirements, and receiving compliant samples for verification / testing.

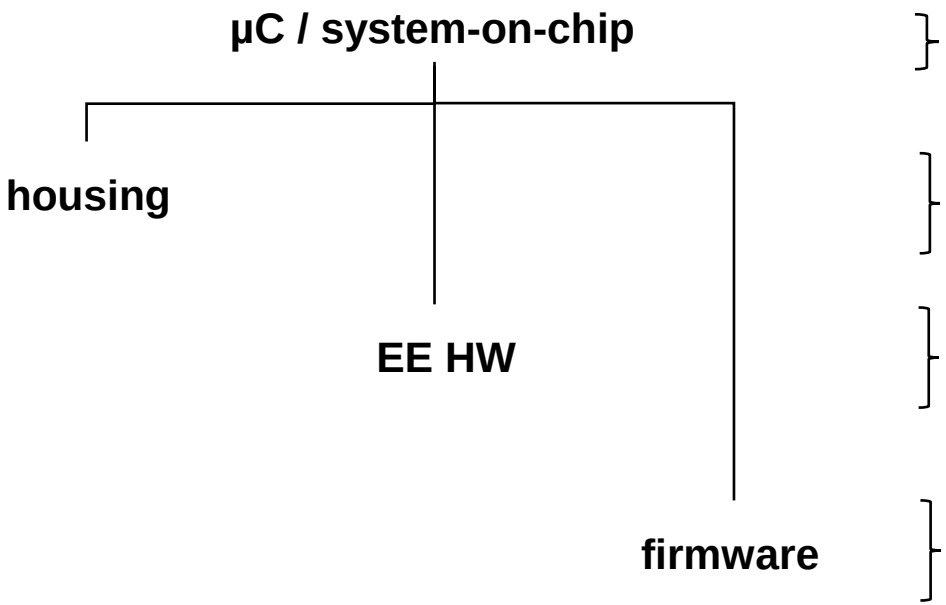
Technical Scope of the PRM/PAM (2/3)

- Why Automotive SPICE as a PAM does not describe a top-down product hierarchy… and therefore can be applied at many levels by means of assessing different “process instances”



Technical Scope of the PRM/PAM (3/3)

- How to assess a non-fundamental HW element such as µC/ system-on-chip:



Automotive SPICE® SYS.x processes

intacs® MEE processes

Automotive SPICE® HWE processes
or intacs® **Hardware SPICE** with
Functional Safety & Cybersecurity

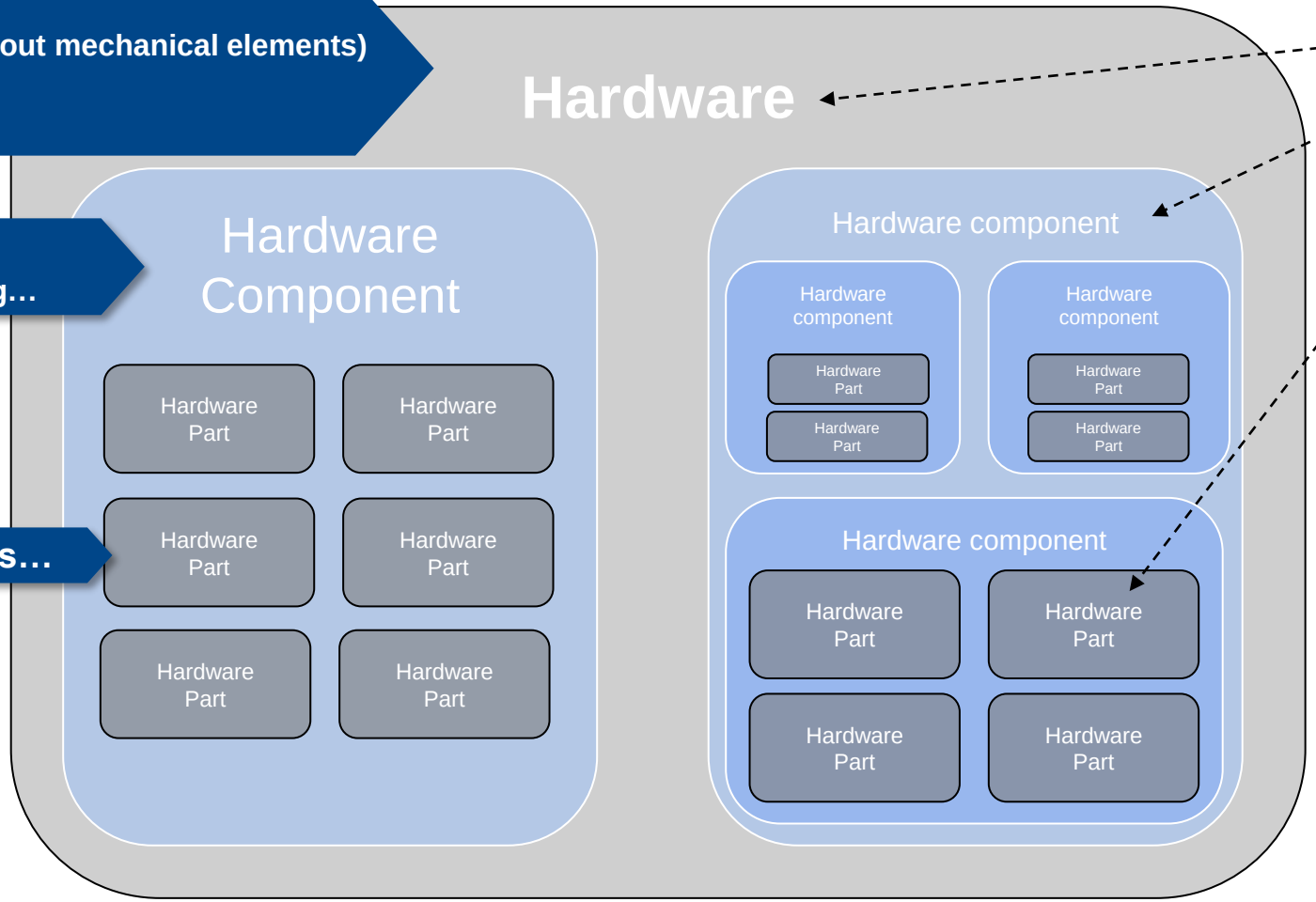
Automotive SPICE® SWE.x processes

Terminology: “Hardware component” and “Hardware element”

Controller device supplier: PCB (without mechanical elements)
Semiconductor: chip

Functional blocks
e.g. power supply, voltage monitoring…

e.g. transistors, resistors, diodes…



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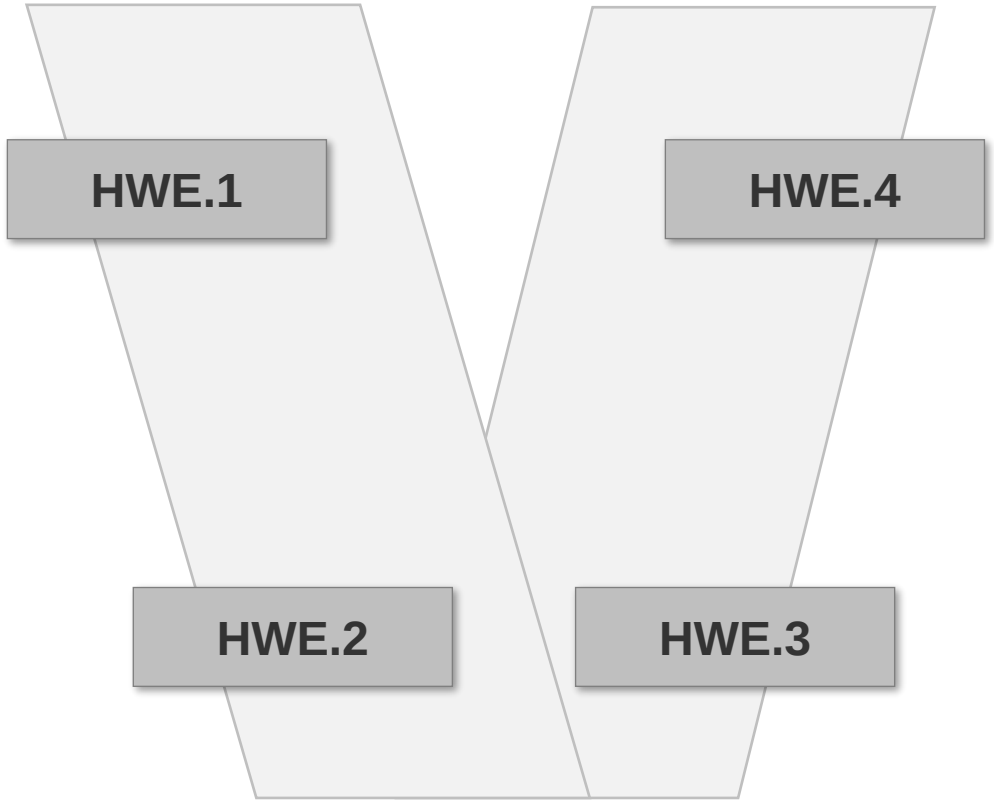
The four HWE processes

Hardware Requirements Analysis

Transform the hardware-related system requirements and hardware-related system architectural design into a set of hardware requirements

Hardware Design

Provide an evaluated design that is suitable for manufacturing and to derive production-relevant data.



Verification against Hardware Requirements

Ensure that the complete hardware is verified to provide evidence for compliance with the hardware requirements.

Verification against Hardware Design

Ensure that the HW is verified to provide evidence for compliance with the hardware design.

HWE.1 – Hardware Requirements Analysis

- **Input from the system level**
  - SYS.2: HW-relevant system requirements
  - SYS.3: relevant interface definitions (HW-SW, HW-mechanics)

- **Hardware requirements**
  - e.g. Lifetime & mission profile, temperature, maximum hardware heat dissipation, voltage impulse responsiveness to crank, start-stop, drop-out, load dump
  - Input from e.g. safety analyses

- **impact on the operating environment**
  - e.g. the mounting space and position, heat dissipation, optical/illuminations

BP1: Specify hardware requirements
BP2: Structure hardware requirements
BP3: Analyse hardware requirements
BP4: Analyse the impact on the operating environment
BP5: Ensure consistency and establish bidirectional traceability
BP6: Communicate agreed hardware requirements

HWE.2 – Hardware Design

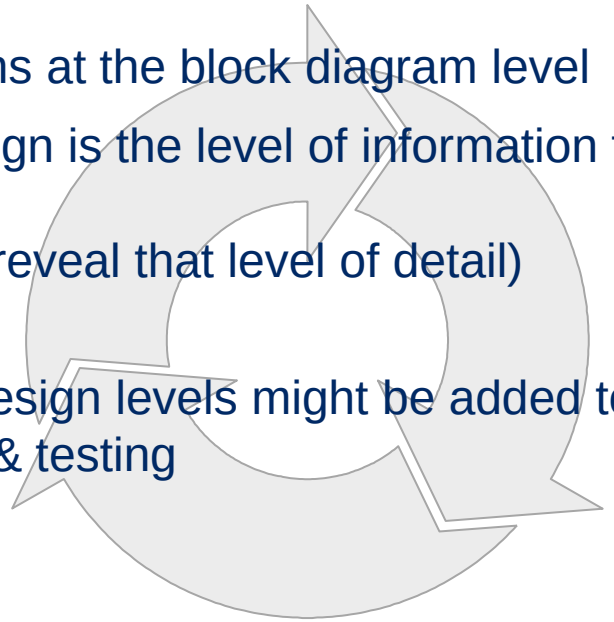
- **Hardware architecture**
  - Block diagrams with functional blocks (HW components)
  - Including e.g. supply concept, EMV concept …

- **Hardware detailed design**
  - Schematic, layout, BOM (HW part identification)
  - Industry requirements (e.g. AEC-Q, REACH) design rules, procurement criteria, etc.
  - Dynamics, e.g. power-up and power-down sequences, debouncing time intervals, etc.
  - Design analyses (e.g. safety analyses)
  - Production data (BOM, Gerber data, special characteristics, etc.)

BP1: Specify the hardware architecture
BP2: Specify the hardware design
BP3: Specify dynamic aspects
BP4: Analyse the hardware architecture and the hardware detailed design
BP5: Ensure consistency and establish bidirectional traceability
BP6: Communicate agreed hardware architecture and hardware detailed design

HWE.2 – Hardware Design
Rationale for not having an extra HW Architectural Design process

- **In practice**
  1. HW architectural design begins at the block diagram level
  2. Subsequent detailed HW design is the level of information from which physical HW instances can be created
     (initial block diagrams do not reveal that level of detail)
  3. Iterations:
     technical details from lower design levels might be added to block diagram in order to support architecture-level verification & testing



- **Further:**
  - A PRM/PAM is not a lifecycle model
  - A lifecycle model defines e.g. a logical order of phases, activities, workflows, and parallelization

HWE.3 – Verification Against Hardware Design

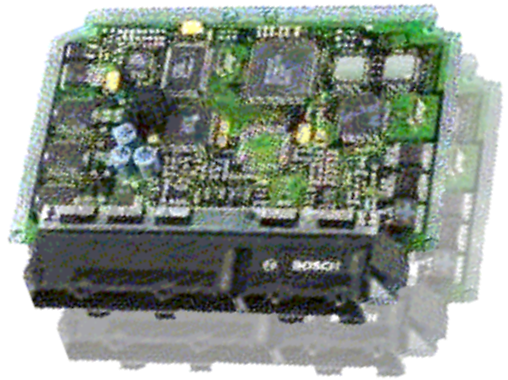
- Verification measure: e.g. testing, measurements, simulations, calculations, reviews…
- No integration: PCB is populated
- Hardware components are stepwise verified using measurement points
- Interface test to software and mechanical interface test on system level (SYS.4)

- **Receiving production data-compliant samples**

"Production interface"
(no production process in the Hardware SPICE)

BP1: Specify verification measures for the verification against hardware design
BP2: Ensure use of compliant samples
BP3: Select verification measures
BP4: Verify hardware design
BP5: Ensure consistency and establish bidirectional traceability
BP6: Summarise and communicate results

HWE.3 – Verification Against HW Design
Rationale for not introducing the notion of “integration testing”



- **Integration is commonly understood as**
  - stepwise assembly of a product
  - and performing tests along, or in between, the assembly steps.

- **This notion is not always applicable to hardware development:**
  - The hardware mostly completely assembled,
  - then hardware component-level testing is performed on the fully assembled PCB
    (by e.g. using measuring points inside the hardware components to test the inputs and outputs with variations)
  - Testing of a single HW component always includes the testing of the interfaces
    (Reason: such tests need electrical input signals and output load)

- **Conclusion: there is no meaningful conceptual distinction between**
  - ‘testing a single HW component in isolation’
  - and ‘testing interfaces between HW components’

HWE.4 – Verification Against Hardware Requirements

- **Analogous to HWE.3**

- **Goal here:**
  - Verify that the pure hardware works properly
  - This means excluding software and mechanics (…however, mechanics and / or software may serve as the test infrastructure...)

BP1: Specify verification measures for the verification against hardware requirements
BP2: Ensure use of compliant samples
BP3: Select verification measures
BP4: Verify hardware
BP5: Ensure consistency and establish bidirectional traceability
BP6: Summarise and communicate results

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Actual achievements

- **Continuous updating**
  - Reflecting change requests from the community (trainers assessors)
  - Collecting daily experiences from the Automotive SPICE HWE or the independent intacs® Hardware SPICE PAM assessments

- **Assessors benefits:**
  - intacs® publications of
    - training syllabi
    - training materials
  - Full acceptance of Hardware SPICE assessments as EE
  - Cross-references to ISO 26262-11:2018

Future – outlook to the next intacs® Hardware SPICE

- **Continuous updating**
  - Reflecting change requests from the community (trainers assessors)
  - Collecting daily experiences from the Automotive SPICE HWE or the independent intacs® Hardware SPICE PAM assessments

- **Assessors benefits:**
  - intacs® publications of
    - training syllabi
    - training materials
  - Full acceptance of Hardware SPICE assessments as EE
  - Mappings to ISO 21434 (cybersecurity)

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DO YOU HAVE ANY QUESTIONS?

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iNTACS e.V. | Herderstr. 7 | 51147 Cologne | Germany | www.intacs.info | office@intacs.info